IN THE CLAIMS

Please cancel claim 1 without prejudice.

Please add claims 26-50 as indicated below.

1. – 25 (Cancelled).

26. (New) A device, comprising:

a clock circuit to receive an input clock signal and an enable signal and to generate a pre-charge pulsed clock signal and an evaluate pulsed clock signal based on the input clock signal and the enable signal, to pre-charge and evaluate a circuit respectively; and

a pre-charge circuit coupled to the clock circuit to receive the pre-charge pulsed clock signal and the enable signal to pre-charge the circuit, while the circuit is not being evaluated via the evaluate pulsed clock signal,

wherein the enable signal, when de-activated, causes the pre-charge circuit to continue pre-charging the circuit regardless of states of the pre-charge pulsed clock signal.

27. (New) The device of claim 26, wherein the enable signal, when de-activated, prevents the circuit from being evaluated, regardless of states of the evaluate pulsed clock signal.

28. (New) The device of claim 26, further comprising a latch circuit coupled to the clock circuit and the pre-charge circuit, to store the enable signal for the clock circuit and the pre-charge circuit based on the input clock signal.

29. (New) The device of claim 28, wherein the latch circuit stores the enable signal during a positive clock cycle of the input clock signal.

30. (New) The device of claim 26, wherein the pre-charge circuit comprises:

an inverter to receive the enable signal to provide a complement of the enable signal;

and

an AND gate coupled to an output of the inverter and an output of the clock circuit, the AND gate receiving the pre-charge pulsed clock signal from the clock circuit and the complemented enable signal from the inverter to generate a pre-charge signal to pre-charge the circuit.

31. (New) The device of claim 26, wherein the clock circuit comprises a first input, a second input, and a third input, the first input receiving the input clock signal, the second input receiving a complement of the input clock signal via an inverter, and the third input receiving the enable signal respectively.

32. (New) The device of claim 26, wherein the clock circuit comprises a first and a second clock generator to generate the pre-charge and evaluate pulsed clock signals respectively based on the enable signal and the input clock signal.

33. (New) The device of claim 32, wherein at least one of the first and second clock generators comprises:

a first input to receive the enable signal;

a second input to receive the input clock signal;

an output to provide a pulsed clock signal;

a first p-type transistor having a source, drain, and gate terminals, the source terminal being coupled to a power supply and the drain terminal being coupled to a node to provide the pulsed clock signal at the output;

a second p-type transistor having a source, drain, and gate terminals, the source terminal being coupled to the power supply, the drain terminal being coupled to the node, the gate terminal being coupled to the output;

a NOR gate coupled to the node to receive the enable signal received at the first input; and

a first n-type transistor coupled to the node to receive the input clock signal at the second input, the pulsed clock signal being generated at the node, which is provided at the output.

34. (New) The device of claim 33, wherein the second p-type transistor performs a function of retaining a potential level at the node.

35. (New) The device of claim 33, wherein the NOR gate further receives the input clock signal from the input, the received input clock signal being delayed by a predetermined gate-wide cycles.

36. (New) The device of claim 35, wherein the delayed input clock signal is delayed via one or more inverters.

37. (New) The device of claim 33, wherein the clock generator further comprises a second n-type transistor having a source, drain, and gate terminals, the drain terminal being coupled to the node, the gate terminal being coupled to an output of the NOR gate, and the source terminal being coupled to the drain terminal of the first n-type transistor.

38. (New) The device of claim 33, wherein the clock generator further comprises an inverter coupled to the node and the output to provide a complement of the signal of the node.

39. (New) The device of claim 33, wherein the gate terminal of the first p-type transistor receives the pulsed clock signal from the output delayed by a predetermined gate-wide cycles.

40. (New) The device of claim 39, wherein the delayed pulsed clock signal is delayed via one or more inverters.

41. (New) A method, comprising:

receiving an enable signal and an input clock signal; and

generating a pre-charge pulsed clock signal and an evaluate pulsed clock signal in response to the enable signal and the input clock signal, the pre-charge pulsed clock signal and the evaluate pulsed clock signal being sued to pre-charge and evaluate a circuit respectively,

wherein the circuit is pre-charged while it is not evaluated, and wherein the enable signal, when de-activated, causes the circuit to be pre-charge continuously regardless of states of the pre-charge pulsed clock signal.

42. (New) The method of claim 41, further comprising preventing the circuit from being evaluated, when the enable signal is de-activated.

43. (New) The method of claim 41, wherein the circuit is pre-charged via a pre-charge circuit, the pre-charge circuit comprises:

an inverter to receive the enable signal to provide a complement of the enable signal; and

an AND gate coupled to an output of the inverter, the AND gate receiving the pre-charge pulsed clock signal and the complemented enable signal to generate a pre-charge signal to pre-charge the circuit.

44. (New) The method of claim 41, wherein one of the pre-charge pulsed clock signal and the evaluate pulsed clock signal is generated by a clock generator, the clock generator comprises:

a first input to receive the enable signal;

a second input to receive the input clock signal;

an output to provide a pulsed clock signal;

a first p-type transistor having a source, drain, and gate terminals, the source terminal being coupled to a power supply and the drain terminal being coupled to a node to provide the pulsed clock signal at the output;

a second p-type transistor having a source, drain, and gate terminals, the source terminal being coupled to the power supply, the drain terminal being coupled to the node, the gate terminal being coupled to the output;

a NOR gate coupled to the node to receive the enable signal received at the first input; and

a first n-type transistor coupled to the node to receive the input clock signal at the second input, the pulsed clock signal being generated at the node, which is provided at the output.

45. (New) The method of claim 44, wherein the NOR gate further receives the input clock signal from the input, the received input clock signal being delayed by a predetermined gate-wide cycles.

46. (New) The method of claim 45, wherein the delayed input clock signal is delayed via one or more inverters.

47. (New) The method of claim 44, wherein the clock generator further comprises a second n-type transistor having a source, drain, and gate terminals, the drain terminal being coupled to the node, the gate terminal being coupled to an output of the NOR gate, and the source terminal being coupled to the drain terminal of the first n-type transistor.

48. (New) The method of claim 44, wherein the clock generator further comprises an inverter coupled to the node and the output to provide a complement of the signal of the node.

49. (New) The method of claim 44, wherein the gate terminal of the first p-type transistor receives the pulsed clock signal from the output delayed by a predetermined gate-wide cycles.

50. (New) The method of claim 49, wherein the delayed pulsed clock signal is delayed via one or more inverters.